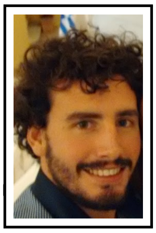

# Dionysios **Diamantopoulos**


PhD · Research Associate · R&D Computer Engineer

*Thalwil, 8800, Zurich Canton, Switzerland*

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| dionysiosdiamantopoulos | dionisis.diamantopoulos | diamantopoulos


***Cover note:*** *Developing innovative digital systems and design tools as well, by following a multi-facet approach is my core belief in the last years of my work experience. A strong research background gives me the analytical framework for simplifying complexity. In the past years I have actively participated in several leading multi-national projects delivering world-class digital systems with highly acknowledged contribution in the realization of reconfigurable and application specific computing. Being passionate about all things to do with silicon bring-up, I am constantly looking to deploy my expertise in world-class R&D computer engineering challenges.*

## Education

**NTUA (Electrical & Computer Engineering - National Technical Univ. of Athens)** *Athens, Greece*

Ph.D. in Computer Science & Engineering *November 2009 - July 2015*

- Dissertation title: “Cross-Layer Rapid Prototyping and Synthesis of Application-Specific and Reconfigurable Many-accelerator Platforms”. Available in **Greek** (280 pages) & **English** (237 pages).
- Advisor: Assoc. Prof. NTUA Dimitrios Soudris.
- Promotion Committee: Assoc. Prof. NTUA D. Soudris, Prof. NTUA K. Pekmestzi, Assis. Prof. NTUA G. Economakos, Assis. Prof. U. Patras G. Theodoridis, Assoc. Prof. NKUA D. Reisis, Prof. RUB M. Hübner and Professor TUC D. Pnevmatikatos.

**CEID (Computer Engineering & Informatics - University of Patras)** *Patras, Greece*

M.Eng in Computer Engineering & Informatics *September 2002 - October 2009*

- Diploma Thesis: “Design and Implementation of a dual-processor(RISC) System-on-Chip targeting machine vision algorithms”.
- Advisor: Professor CEID George Alexiou.

## Skills

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| **EDA/CAD** | **FPGAs:** Xilinx EDK/ISE/Vivado/Vivado HLS, Altera Quartus, Actel Libero, Synopsys Synplify, **ASICs:** Synopsys (Design Compiler, Primetime), Cadence (IUS, SOC Encounter, Virtuoso), **Other CADs Tools:** Cadence OrCAD, SPICE, Mentor Modelsim. |
| **Embedded** | Software and hardware development with several MCU and DSP platforms (e.g. Atmel AVR MCU’s, Microchip PIC MCU’s, Texas Instruments DSP’s), Microchip Mplab, AVR studio, ARM Development Studio, Parallanx Basic Stamp. |
| **Control/Test** | Simulink, Xilinx ChipScope Pro, Synopsys Formality. |
| **Prog/ing:** | C, C++, OpenCV, Java, Shell scripting (bash,tcsh,ksh,zsh), GNU make, Cmake, Tcl, Pyhton, MySQL, M ATLAB /Octave, C(OpenMP/MPI). |
| **Version Con.** | DVCS (Mercurial, Git), VCS (CVS, SVN), Trac. |
| **Docum/tion** | TeX (LaTeX), Vim, Kile, Libreoffice, MS Office. |
| **OS’es** | Linux (binary and source-rolling based), FreeBSD and other UNIX variants, Microsoft Windows. |
| **Languages** | Greek (Native language), English (TOEIC, Hellenic-American Union, Score : 805/990, Advanced Level). |

## Professional Experience

**IBM** *Zurich, Switzerland.*

PostDoc Researcher, **IBM Research - Zurich** *September 2017 - Today*

- Transprecision & Energy-efficient Computing.
- Reconfigurable Accelerators for Deep Learning & Machine Learning.
- Near-Memory Computing.
- On-chip Interconnection Networks, Hardware-Software Codesign and High-Level-Synthesis.

**LN2 Hellas - LN2** *Athens, Greece - Washington, U.S.*

Senior R&D Engineer, **LN2** *January 2017 - August 2017*

- FPGA/ASIC and SoC IP for unmatched, state-of-the art designs for communications, broadcast, signal processing, and magneto-optical recording and storage systems.
- FEC accelerators for IoT/V2V/V2X communication systems.

### Military Service
*Athens, Greece*

SPECIALIZED SCIENTIST - APPLICATION AND SYSTEMS ENGINEER — *March 2016 - December 2016*

- IT Support Center of Hellenic Army **ΚΕ.Π.Υ.Ε.Σ** - Hellenic Army General Staff

### ALMA CIDCIP, si-Cluster Collaborative Research Program
*Athens, Greece*

PRIMARY RESEARCHER, SENIOR HARDWARE DESIGNER — *Jan. 2015 - Jan. 2016*

- VHDL Coding, Architecture Design for FPGA algorithms implementation on image data compression.
- Funded by European Union and the National Strategic Reference Framework (NSRF).
- Co-Supervised by Hellenic Space Technologies and Applications Cluster (si-Cluster).

### MENELAOS, si-Cluster Collaborative Research Program
*Athens, Greece*

PRIMARY RESEARCHER, SENIOR HARDWARE DESIGNER — *Jan. 2015 - Jan. 2016*

- Design, development and ASIC implementation of the appropriate interface electronics of an "IMU" Unit (for space applications).
- Funded by European Union and the National Strategic Reference Framework (NSRF).
- Co-Supervised by Hellenic Space Technologies and Applications Cluster (si-Cluster).

### AEGLE Research Program, An analytics framework for intergrated and personalized healthcare services design.
*Athens, Greece*

RESEARCHER, HARDWARE DESIGNER, SOFTWARE DEVELOPER — *Mar. 2015 - Nov. 2015*

- AEGLE system and services design. Horizon 2020 ICT funded program.
- Design of data access layer. Design of mediation layer. Design of presentation layer.
- Alignment with cloud SOA.

### SEXTANT Research Program, European Space Agency
*Greece, Spain, The Netherlands*

PRIMARY INVESTIGATOR, PHD RESEARCHER, HARDWARE DESIGNER — *01 May 2012 - 31 Dec. 2014*

- Assessment of feasibility and prototyping of integrating orbital imagery to the Simultaneous Localization and Mapping (SLAM) component of the system.
- Project SEXTANT: Extension Activity to SPARTAN (Sparing Robotics Technologies for Autonomous Navigation), funded by European Space Agency (ESA) for the ExoMars programme 2018.

### SPARTAN Research Program, European Space Agency
*Greece, Spain, The Netherlands*

PRIMARY INVESTIGATOR, PHD RESEARCHER, HARDWARE DESIGNER — *01 March 2011 - 30 July 2013*

- Developing reconfigurable hardware accelerators for computational intensive computer vision algorithms, for autonomous robotic navigation.
- Project SPARTAN: Sparing Robotics Technologies for Autonomous Navigation, funded by European Space Agency (ESA) for the ExoMars programme 2018.

### 2PARMA, FP7-ICT Research Program
*Italy, Germany, Belgium, France, Greece*

PHD RESEARCHER, HARDWARE DESIGNER, SOFTWARE DEVELOPER — *01 Sep. 2010 - 31 Dec. 2012*

- PARallel PAradigms and Run-time Management techniques for Many-core Architectures FP7-ICT-2009-4-248716.
- Run-time Management.

### NexGenmmWave, Corallia Collaborative Research Program
*Greece*

SENIOR DIGITAL DESIGNER, PHD RESEARCHER — *01 Sep. 2010 - 31 Dec. 2013*

- Next generation of milliwave radio-coupling (code number: 84702), Project funded by National Ministry of Development and EU.
- Developing and implementing onto FPGA, VHDL IP cores of baseband OFDM transceiver targeting 1Gbps wireless link on LTE/WiMAX backbone networks.

### HiPEAC Research Program, Internship at EPFL
*Switzerland, Greece*

PHD RESEARCHER — *01 Nov. 2010 - 30 Jul. 2011*

- On Providing Dynamic Reliability Improvement in FPGAs, Project funded by HiPEAC.
- Investigating new design techniques for early design space exploration of emerging technologies.

### Science View Company
*Greece*

ACADEMIC TRAINER — *01 Nov. 2010 - 30 Jul. 2011*

- Industrial Seminar, Reconfigurable Architectures and Tools, Project funded by Science View Company.
- Organize teaching material for 60 hours/7 days presentations. Supporting practical excercices (EDA tools and examples).

**MNEMEE, FP7-ICT Research Program** *France, Germany, Greece*

PhD Researcher, Hardware Designer, Software Developer *01 Jan. 2009 - 31 Mar. 2010*

- Memory management technology for adaptive and efficient design of embedded systems, 7th IST Framework, No. 216224, STREP
- ICT-2007.3.3: Embedded Systems Design.

## Academic Experience

**Teaching Assistant** *Athens, Greece*

Microlab, ECE, National Technical University of Athens *Nov. 2009 - Today*

- Microprocessor systems
- Microprocessor systems laboratory
- Digital VLSI Systems
- Introduction to VLSI Systems

**Diploma Thesis co-Advisor** *Athens, Greece*

Microlab, ECE, National Technical University of Athens *Nov. 2009 - Today*

- High-Level-Synthesis of Harris Computer Vision Algorithm onto FPGA, G. Galanis, 2014.
- High level synthesis of the OpenSURF algorithm, K. Faliagkas, 2013
- FPGA Implementation of Computer Vision Algorithms: Application on Landmark Matching Algorithm, C. Ignatios, 2012.
- FPGA Implementation of Computer Vision Algorithms Application on Linear Time Selection Algorithm, G. Tzimpragos, 2012.
- A Methodology and Software Tool for the Performance Evaluation of Embedded Systems, M. Vichos, 2011.

**Referee Service** *International*

International peer-reviewing Journals & Conferences *Nov. 2009 - Today*

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| × IEEE MICRO 2009 | × Transactions on Hipeac 2009 | × DATE 2010 | × ISCAS 2012, 2013 |
| × DATE 2010 | × FPL 2010, 2011, 2012, 2014, 2015 | × ICECS 2010, 2011, 2012 | × JSCS 2012 |
| × ISCC 2010 | × PATMOS 2010 | × JOLPE 2010 | |

## Extracurricular Activity

**Hellenic Linux User Group & Patras Linux User Group** *Patras, Athens*

Member *Jan. 2003 - PRESENT*

- Gained expertise in Open Source / Free software.
- Participated on a lot of "hackathlon" competitions.
- Held several hacking competitions / tutorials / presentations non-profit, just for education.

**Linux Inside Magazine** *Athens*

Author *May 2012*

- Co-authored a complete hands-on tutorial on Robotic Operating System (ROS), Issue 8, pages 68-69.
- Covered installation procedure of ROS libraries to Ubuntu Linux and basic programming aspects for creating a basic node scheme.

## Honors & Awards

### International

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| 2018 | **Featured Poster Award**, COOL Chips 21, For the paper entitled: "ecTALK: Energy efficient coherent transprecision accelerators - The bidirectional long short-term memory neural network case". | *Yokohama, Japan* |
| 2013 | **2nd Place**, Cadence Design Systems, CDNLive EMEA, Cadence Thesis Contest for Automotive Embedded Systems. | *Munich, Germany* |
| 2013 | **Best Paper**, 4th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures (PARMA) January 23. | *Berlin, Germany* |
| 2013 | **Finalist**, University Booth on Conference IEEE International Conference on Design Automation and Test in Europe (DATE) | *Grenoble, France* |
| 2013 | **2nd Place**, Journal Invitation "ACM Transactions on Embedded Computing Systems (TECS)", "Workshop on Virtual Prototyping of Parallel and Embedded Systems (VIPES)" | *International* |
| 2012 | **Finalist**, University Booth on Conference IEEE International Conference on Design Automation and Test in Europe (DATE) | *Dresden, Germany* |

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| 2011 | **Finalist**, HiPEAC: Grant for International Summer School (7 days) on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, July. | *Fiuggi, Italy* |

### Domestic

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|---|---|---|
| 2004 | **Finalist**, Excellence award and 1000€ prize for being accepted at the Computer Engineering and Informatics Department (CEID) on top ten of students, according to GPA grade, from Commercial Bank of Greece. | *Athens, Greece* |
| 2000 & 2001 | **Finalist**, Excellence award from Greek minister of education. | *Athens, Greece* |

## Publications

### Book Chapters

| | | |
|---|---|---|
| 2014 | **1**, Konstantinos Tatas, Kostas Siozios, Dimitrios Soudris, Axel Jantsch, "Designing 2D and 3D Network-on-Chip Architectures", Authors refer on "Chapter 9, On Designing 3-D Platforms" that: "This chapter was contributed by D. Diamantopoulos, Kostas Siozios, George Economakos, and Dimitrios Soudris of the School of ECE, National Technical University of Athens.", pp.209-236, doi: 10.1007/978-1-4614-4274-5_9, Springer. | *2014* |

### Peer Reviewed International Journals

| | | |
|---|---|---|
| 2017 | **9**, I. Koutras, K. Maragos, D. Diamantopoulos, K. Siozios, D. Soudris, "On supporting rapid prototyping of embedded systems with reconfigurable architectures," Integration, Elsevier, Volume 58, pp.91,100 doi: 10.1016/j.vlsi.2017.02.007. | *June 2017* |
| 2016 | **8**, C. Kachris, D. Diamantopoulos, G. Ch. Sirakoulis, D. Soudris, "An FPGA-based Integrated MapReduce Accelerator Platform," Journal of Signal Processing Systems, Springer, pp.1,13 doi: 10.1007/s11265-016-1108-7. | *February 2016* |
| 2015 | **7**, D. Diamantopoulos, S. Xydis, K. Siozios, D. Soudris, "Mitigating Memory-induced Dark Silicon in Many-Accelerator Architectures," IEEE Computer Architecture Letters , vol.PP, no.99, pp.1,1 doi: 10.1109/LCA.2015.2410791. | *March 2015* |
| 2015 | **6**, D. Diamantopoulos, K. Siozios, S. Xydis, D. Soudris. "GENESIS: Parallel Application Placement onto Reconfigurable Architectures (Invited for the Special Issue on Runtime Management)." ACM Transactions on Embedded Computing Systems (TECS) vol. 14, no. 1: 18, doi: 10.1145/2629651. | *January 2015* |
| 2014 | **5**, I. Kostavelis, L. Nalpantidis, E. Boukas, M. Aviles Rodrigalvarez, I. Stamoulias, G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris, A. Gasteratos. "SPARTAN: Developing a vision system for future autonomous space exploration robots." Journal of Field Robotics vol. 31, no. 1, pp.107-140. doi:10.1002/rob.21484. | *January 2014* |
| 2014 | **4**, E. Sotiriou-Xanthopoulos, D. Diamantopoulos, K. Siozios, G. Economakos, D. Soudris. "A framework for rapid evaluation of heterogeneous 3-D NoC architectures." Elsevier Microprocessors and Microsystems vol. 38, no. 4, pp. 292-303,doi:10.1016/j.micpro.2013.09.003. | *June 2014* |
| 2014 | **3**, D. Diamantopoulos, E. Sotiriou-Xanthopoulos, K. Siozios, G. Economakos, D. Soudris. "Plug&Chip: A Framework for Supporting Rapid Prototyping of 3D Hybrid Virtual SoCs". ACM Transactions on Embedded Computing Systems (TECS), vol. 13, no. 5s, Article 168, pp. 1-25, 25 pages, doi:10.1145/2661634. | *December 2014* |
| 2012 | **2**, D. Diamantopoulos, K. Siozios and D. Soudris, A Framework for Performing Rapid Evaluation of 3-D SoCs, IET Electronics Letters, pp. 679 - 681, doi:10.1049/el.2012.1321. | *June 2012* |
| 2012 | **1**, D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, A Systematic Methodology for Reliability Improvements on SoC-based Software Defined Radio Systems, VLSI Design, Vol. 2012, Article ID 784945, doi:10.1155/2012/784945. | *January 2012* |

## Peer Reviewed International Conference Publications

| | | |
|---|---|---|
| Sep. 2019 | **23**, Gagandeep Singh, D. Diamantopoulos, Christoph Hagleitner, Sander Stuijk, Henk Corporaal, 'NARMADA: Near-Memory Horizontal Diffusion Accelerator for Scalable Stencil Computations", 29th International Conference on Field Programmable Logic and Applications (FPL), pp. 263-269, 2019. | *Barcelona, Spain* |
| Jul. 2019 | **22**, Gagandeep Singh, D. Diamantopoulos, Sander Stuijk, Christoph Hagleitner, Henk Corporaal, 'Low Precision Processing for High Order Stencil Computations", International Conference on Embedded Computer System, pp. 403–415, 2019. | *Samos, Greece* |
| Jul. 2019 | **21**, D. Diamantopoulos, C. Hagleitner, 'HelmGemm: Managing GPUs and FPGAs for transprecision GEMM workloads in containerized environments", IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019. | *New York, USA* |
| Mar. 2019 | **20**, J.van Lunteren, R. Luijten, D. Diamantopoulos, F. Auernhammer, C. Hagleitner, L. Chelini, S. Corda, G. Singh, 'Coherently Attached Programmable Near-Memory Acceleration Platform and its application to Stencil Processing", DATE, pp. 668-673, 2019. | *Florence, Italy* |
| Dec. 2018 | **19**, D. Diamantopoulos, C. Hagleitner:, 'A System-level Transprecision FPGA Accelerator for BLSTM with On-chip Memory Reshaping", International Conference on Field-Programmable Technology (FPT), 2018 | *Naha, Okinawa, Japan* |
| Apr. 2018 | **18**, D. Diamantopoulos, H. Giefers, C. Hagleitner:, 'ecTALK: Energy efficient coherent transprecision accelerators - The bidirectional long short-term memory neural network case", IEEE Symposium in Low-Power and High-Speed Chips (COOL CHIPS), 2018, *Featured Poster Award.* | *Yokohama, Japan* |
| May 2018 | **17**, H. Giefers and D. Diamantopoulos, 'Extending the POWER Architecture with Transprecision Co-Processors", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1-5 2018. | *Florence, Italy* |
| Jul. 2015 | **16**, D. Diamantopoulos, C. Kachris. "High-level Synthesizable Dataflow MapRe-duce Accelerator for FPGA-coupled Data Centers", Embedded Computer Systems (SAMOS), 2015 International Conference on. | *Samos, Greece* |
| Mar. 2015 | **15**, D. Diamantopoulos, S. Xydis, K. Siozios, D. Soudris. "Dynamic memory management in Vivado-hls for scalable many-accelerator architectures." In Applied Reconfigurable Computing (ARC), pp. 117-128. Springer International Publishing. | *Bochum, Germany* |
| Mar. 2015 | **14**, E. Sotiriou-Xanthopoulos, D. Diamantopoulos, G. Economakos. "Evaluation of High-Level Synthesis Techniques for Memory and Datapath Tradeoffs in FPGA Based SoC Architectures." In Applied Reconfigurable Computing (ARC), pp. 321-330. Springer International Publishing. | *Bochum, Germany* |
| Mar. 2015 | **13**, K. Siozios, P. Figuli, H. Sidiropoulos, C. Tradowsky, D. Diamantopoulos, K. Maragos, S. Percy Delicia, D. Soudris, J. Becker. "TEAChER: TEach AdvanCEd Reconfigurable Architectures and Tools." In Applied Reconfigu-rable Computing (ARC), pp. 103-114. Springer International Publishing. | *Bochum, Germany* |
| Mar. 2015 | **12**, G. Lentaris, I. Stamoulias, D. Diamantopoulos, K. Maragos, K. Siozios, D. Soudris, M. Aviles Rodrigalvarez, M. Lourakis, X. Zabulis, I. Kostavelis, L. Nalpantidis, E. Boukas, A. Gasteratos, "SPARTAN/SEXTANT/COMPASS: Advancing Space Rover Vision via Reconfigurable Platforms." In Applied Reconfigurable Computing (ARC), pp. 475-486. Springer International Publishing | *Bochum, Germany* |
| Dec. 2014 | **11**, D. Diamantopoulos, G. Economakos, D. Reisis, "Using high-level synthesis to build memory and datapath optimized DSP accelerators," Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on, pp.714,717, doi: 10.1109/ICECS.2014.7050085. | *Marseille, France* |
| Dec. 2013 | **10**, D. Diamantopoulos, C. Economakos, D. Soudris, G. Economakos, "A new design paradigm for floating point DSP applications based on ESL/HLS and FPGAs," Signal Processing and Information Technology (ISSPIT), 2013 IEEE International Symposium on, pp.000404,000409, 12-15, doi: 10.1109/ISSPIT.2013.6781915. | *Athens, Greece* |
| May 2013 | **9**, D. Diamantopoulos, K. Siozios, E. Sotiriou-Xanthopoulos, G. Economakos, D. Soudris, "HVSoCs: A Framework for Rapid Prototyping of 3-D Hybrid Virtual System-on-Chips," Parallel and Distributed Processing Symposium Workshops & PhD Forum (IPDPSW), 2013 IEEE 27th International, pp.2194,2199, 20-24, doi: 10.1109/IPDPSW.2013.202. | *Boston, Massachusetts U.S.A.* |
| Dec. 2012 | **8**, G. Lentaris, D. Diamantopoulos, G. Stamoulias, K. Siozios, D. Soudris, M.A. Rodrigalvarez, "FPGA-based path-planning of high mobility rover for future planetary missions," Electronics, Circuits and Systems (ICECS), 2012 19th IEEE International Conference on, pp.85,88, doi: 10.1109/ICECS.2012.6463793. | *Seville, Spain* |

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| Jun. 2012 | **7**, D. Diamantopoulos, K. Siozios, G. Lentaris, D. Soudris, M.A. Rodrigalvarez, “SPARTAN project: On profiling computer vision algorithms for rover naviga-tion,” Adaptive Hardware and Systems (AHS), 2012 NASA/ESA Conference on, pp.174,181, doi: 10.1109/AHS.2012.6268647. | *Fraunhofer Institute for Integrated Circuits IIS, Erlangen, Germany* |
| Aug. 2012 | **6**, G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris, M.A. Rodrigalvarez, “Hardware implementation of stereo correspondence algorithm for the Exo-Mars mission,” Field Programmable Logic and Applications (FPL), 2012 22nd International Conference on , pp.667,670, doi: 10.1109/FPL.2012.6339173. | *Oslo, Norway* |
| Dec. 2011 | **5**, D. Diamantopoulos, P. Galiatsatos, A. Karachalios, G. Lentaris, D. Reisis, D. Soudris, “Configurable baseband digital transceiver for Gbps wireless 60 GHz communications,” Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference on, pp.192,195, doi: 10.1109/ICECS.2011.6122246. | *Beirut, Lebanon* |
| Dec. 2011 | **4**, E. Sotiriou-Xanthopoulos, D. Diamantopoulos, G. Economakos, D. Soudris, “Design and experimentation with low-power morphable multipliers,” Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Confe-rence on , vol., no., pp.752,755, doi: 10.1109/ICECS.2011.6122383. | *Beirut, Lebanon* |
| Jun. 2011 | **3**, K. Siozios, D. Diamantopoulos, I. Kostavelis, E. Boukas, L. Nalpantidis, D. Soudris, A. Gasteratos, M. Aviles, I. Anagnostopoulos, “SPARTAN project: Efficient implementation of computer vision algorithms onto reconfigurable platform targeting to space applications,” in Proceedings of the 6th Internatio-nal Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), doi:10.1109/ReCoSoC.2011.5981524, pp.1,9, June 2011. | *Montpellier, France* |
| Jul. 2011 | **2**, D. Diamantopoulos, K. Siozios, S. Xydis, D. Soudris, “Thermal optimization for micro-architectures through selective block replication,” Embedded Computer Systems (SAMOS), 2011 International Conference on, pp.59,66, doi: 10.1109/SAMOS.2011.6045445. | *Samos, Greece* |
| Apr. 2011 | **1**, D. Diamantopoulos, K. Siozios, D. Bekiaris, D. Soudris, “A novel methodology for architecture-level exploration of 3D SoCs,” Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 2011 6th International Conference on, pp.1,6, doi: 10.1109/DTIS.2011.5941425. | *Athens, Greece* |

## International Workshops

| | | |
|---|---|---|
| Aug. 2015 | **14**, D. Diamantopoulos, C. Kachris and D. Soudris, “MapReduce FPGA Acceleration for High Performance Computing Machines”, Workshop on Reconfigurable Computing for HPC and HPDA (ReC4P). | *London, UK* |
| Jan. 2015 | **13**, D. Diamantopoulos, I. Galanis, K. Siozios, G. Economakos, and D. Soudris, “A Framework for Rapid System-Level Synthesis Targeting to Reconfigurable Platforms”, Workshop on Reconfigurable Computing (WRC). | *Amsterdam, The Netherlands* |
| May 2013 | **12**, D. Diamantopoulos, K. Siozios, E. Sotiriou-Xanthopoulos, G. Economakos and D. Soudris, “HVSoCs: A Framework for Rapid Prototyping of 3-D Hybrid Virtual System-on-Chips”, Workshop on Virtual Prototyping of Parallel and Embedded Systems (VIPES). | *Boston, U.S.A.* |
| Mar. 2013 | **11**, D. Diamantopoulos, P. Galiatsatos, A. Karachalios, G. Lentaris, D. Reisis and D. Soudris, “A Reconfigurable Baseband Architecture for Gbps Wireless 60 GHz Communications”, Fifth Friday Workshop on Designing for Embedded Parallel Computing Platforms (DEPCP). | *Grenoble, France* |
| Jan. 2013 | **10**, G. Lentaris, D. Diamantopoulos, K. Siozios, I. Stamoulias, I. Kostavelis, E. Boukas, L. Nalpantidis, D. Soudris, A. Gasteratos, and M. Aviles, “SPARTAN: Efficient Implementation of Computer Vision Algorithms for Autonomous Rover Navigation”, Workshop on Reconfigurable Computing (WRC) . | *Berlin, Germany* |
| Jan. 2013 | **9**, G. Lentaris, I. Stamoulias, D. Diamantopoulos, K. Siozios, and D. Soudris, “An FPGA implementation of the SURF algorithm for the ExoMars programme”, Workshop on Reconfigurable Computing (WRC). | *Berlin, Germany* |
| Jan. 2013 | **8**, D. Diamantopoulos, K. Siozios, and D. Soudris, “A Framework for Performing Fault-Tolerant Placement Based on Genetic Algorithm”, Workshop on Reconfigurable Computing (WRC). | *Berlin, Germany* |
| Mar. 2013 | **7**, D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, “A genetic algorithm-based FPGA placer for multi-core processors”, Fifth Friday Workshop on Designing for Embedded Parallel Computing Platforms (DEPCP). | *Grenoble, France* |

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| Mar. 2013 | **6**, D. Diamantopoulos, K. Siozios, I. Stamoulias, G. Lentaris, D. Soudris and M. Aviles, “Towards Computer Vision FPGA Acceleration”, DATE Friday Workshop on Reconfigurable Computing (Configcomp). | *Grenoble, France* |
| Jan. 2013 | **5**, D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, “A Framework for Supporting Parallel Application Placement onto Reconfigurable Platforms”, Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (PARMA). | *Berlin, Germany* |
| Sep. 2012 | **4**, K. Siozios, H. Sidiropoulos, D. Diamantopoulos, P. Figuli, D. Soudris, M. Hubner and J. Becker, “On Designing Self-Aware Reconfigurable Platforms”, Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS), pp. 14-17. | *Oslo, Norway* |
| Mar. 2012 | **3**, D. Diamantopoulos, G. Lentaris, K. Siozios, D. Soudris and M. Aviles, “Towards Accelarating Computer Vision Algorithms Targeting to Space Applications with a Heterogeneous Platform”, Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications at DATE 2012, Germany, 2012. | *Dresden, Germany* |
| Mar. 2011 | **2**, K. Siozios, D. Diamantopoulos, H. Sidiropoulos, A. Papanikolaou, and D. Soudris, “Rapid Evaluation of 3-D Interconnection Schemes”, DATE 2011 3D Integration Workshop, Grenoble, 2011, France. | *Grenoble, France* |
| Sep. 2011 | **1**, M. Aviles, K. Siozios, D. Diamantopoulos, L. Nalpantidis, I. Kostavelis, E. Boukas, D. Soudris and A. Gasteratos, “A Co-design Methodology for Implementing Computer Vision Algorithms for Rover Navigation onto Reconfigurable Hardware”, Workshop on Computer Vision on Low-Power Reconfigurable Architectures, International Conference on Field Programmable Logic and Applications. | *Chania, Greece* |

### Other Publications

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|---|---|---|
| Mar. 2012 | **1**, D. Diamantopoulos, G. Lentaris, A. Douklias, K.Siozios, D.Soudris, “Implementation Trade-offs of Computer Vision Algorithms on Reconfigurabe Computing Targeting to Space Applications”, THE SPARTAN PROJECT, Panhellenic Conference on Electronics and Telecommunications (PACET2012). | *Thessaloniki, Greece* |

## Membership

| | | |
|---|---|---|
| 2015-Tod. | **Member**, Institute of Electrical and Electronics Engineers (IEEE) | *International* |
| 2004-2015 | **Student Member**, Institute of Electrical and Electronics Engineers (IEEE) | *International* |
| 2009-2015 | **Student Member**, Association for Computing Machinery (ACM) | *International* |
| 2009-Tod. | **Member**, European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC) | *European Union* |
| 2009-Tod. | **Core Member**, Technical Chamber of Greece (TEE) | *Greece* |

## External Activities

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|---|---|---|
| 2019-Tod. | **Member**, Sagitta Sailing Team | *Zurich, Switzerland* |
| 2016-Tod. | **Member**, Sailing Spot, Piraeus Sailing Club (IOP) | *Piraeus, Greece* |
| 2015-2016 | **Member**, Match Race Academy Sailing Team, Yacht Club of Greece (YCG) | *Piraeus, Greece* |
| 2014-2016 | **Member**, SAPPAZ Marathon Running Team | *Athens, Greece* |
| 2013-2014 | **Member**, Hellenic Offshore Racing Club, participation in offshore sailing races. | *Piraeus, Greece* |
| 1999-2002 | **Member**, NASP NESTOR Sailing Team | *Pylos, Greece* |
| Always | **Passionate**, Free-diving, Spearfishing | *Pylos, Greece* |